

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Applicant	:	V. K. JaiPrakash, et al.	)	Examiner:
			)	TBA
Serial No.	:	TBA	)	
			)	
Filed	:	Filed Herewith	)	Art Unit
			)	Unknown
For	:	DRAM VERTICAL TRANSISTOR AND	)	
		TRENCHCAPACITOR MEMORY CELLS	)	
		AND METHOD OF FABRICATION	)	

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INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application  
Commissioner For Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

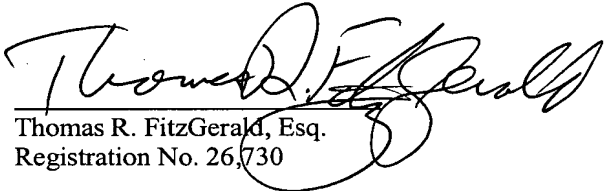
Dear Sir:

Pursuant to 37 CFR §1.97 - §1.98, Applicants hereby bring to the attention of the United States Patent and Trademark Office, the references listed on the attached Form PTO-1449. Copies are not included because the cited references were cited by the USPTO in the parent application identified on page 1 of the specification.

Respectfully submitted,

Date

7/11/03

  
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional).      <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

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